THAT WHICH IS CLAIMED IS:

1. An integrated circuit comprising:

a substrate;

a first dielectric layer adjacent said substrate;

at least one trench in said first dielectric layer;

a liner comprising metal within said at least one trench;

a first conductive region comprising copper within said at least one trench;

a cap layer comprising metal on said first conductive region;

a second dielectric layer over said first conductive region and said cap layer;

a dielectric etch stop and diffusion barrier layer over said second dielectric layer;

a via over said first conductive region and through said second dielectric layer and said cap layer;

a diffusion barrier layer on sidewalls of said via;

an alloy seed layer comprising copper and at least one of tantalum, molybdenum, chromium, and tungsten over said diffusion barrier, said alloy seed layer also over said dielectric etch stop and diffusion barrier layer, said alloy seed layer in contact with said first conductive region; and

a second conductive region comprising copper over said alloy seed layer.

2. An integrated circuit according to Claim 1 wherein said diffusion barrier layer is conductive.

3. An integrated circuit comprising

a substrate;

a first dielectric layer adjacent said substrate;

at least one trench in said first dielectric layer;

a liner comprising metal within said at least one trench;

a first conductive region comprising copper within said at least one trench;

a cap layer on said first conductive region;

a second dielectric layer over said first conductive region and said cap layer;

a dielectric etch stop and diffusion barrier layer over said second dielectric layer;

a via over said first conductive region and through said second dielectric layer and said cap layer;

a conductive diffusion barrier on sidewalls of said via;

an alloy seed layer comprising copper over said conductive diffusion barrier, said alloy seed layer also over said dielectric etch stop and diffusion barrier layer, said alloy seed layer in contact with said first conductive region; and

a second conductive region comprising copper over said alloy seed layer.

4. An integrated circuit according to Claim 3 wherein said alloy seed layer comprises copper and at least one of tantalum, molybdenum, chromium, and tungsten.

5. An integrated circuit according to Claim 3 wherein said cap layer comprises metal.

6. An integrated circuit comprising

a substrate;

a first dielectric layer adjacent said substrate;

at least one trench in said first dielectric layer;

a liner comprising metal within said at least one

trench;

a first conductive region comprising copper within said at least one trench;

a cap layer on said first conductive region;

a second dielectric layer over said first conductive region and said cap layer;

a dielectric etch stop and diffusion barrier layer over said second dielectric layer;

a via over said first conductive region through said second dielectric layer and said cap layer;

a diffusion barrier layer on sidewalls of said via;

an alloy seed layer comprising copper over said second diffusion barrier layer, said alloy seed layer also over said dielectric etch stop and diffusion barrier, said alloy seed layer in contact with said first conductive region; and

a second conductive region comprising copper over said alloy seed layer.

7. An integrated circuit comprising:

a substrate;

a first dielectric layer over said substrate;

at least one trench in said first dielectric layer;

a liner comprising metal within said at least one trench;

a first conductive region comprising copper within said at least one trench;

a cap layer on said first conductive region and comprising at least one of palladium and platinum;

a dielectric etch stop and diffusion barrier layer over said cap layer;

a solid solution at the interface of said first conductive region and said cap layer;

a second dielectric layer over said first conductive

region and said cap layer;

a second dielectric etch stop and diffusion barrier layer over said second dielectric layer;

a via over said first conductive region through said second dielectric layer and through said cap layer;

a third diffusion barrier on the sidewalls of said via;

an alloy seed layer comprising copper and at least one of tantalum, molybdenum, chromium, and tungsten formed over said second dielectric etch stop and diffusion barrier layer, said alloy seed layer also over said third diffusion barrier formed on the sidewalls of said via;

said alloy seed layer in contact with said underlying first conductive region; and

a second conductive region comprising copper over said alloy seed layer.

8. An integrated circuit comprising:

a substrate;

a first dielectric layer over said substrate;

at least one first trench formed in said first dielectric layer;

a liner comprising metal formed in said at least one first trench;

a first conductive region comprising copper formed within said at least one first trench forming an interconnect;

a second dielectric layer over said first conductive region with a dual-damascene type opening therein;

a first diffusion barrier over via and second trench opening sidewalls of said dual-damascene type opening;

a second diffusion barrier is over horizontal surfaces of the second trench opening; and

said first diffusion barrier being a different material than said second diffusion barrier.

9. An integrated circuit according to Claim 8 further comprising an alloy seed layer over said first and second diffusion barriers.

10. An integrated circuit according to Claim 9 wherein said alloy seed layer comprises copper and at least one of tantalum and chromium.

11. An integrated circuit according to Claim 8 further comprising a cap layer comprising at least one of palladium and platinum over said first conductive region.

12. An integrated circuit according to Claim 11 further comprising a dielectric diffusion barrier over said cap layer.

13. An integrated circuit comprising

a substrate;

a dielectric layer over said substrate;

a dual-damascene type opening formed within said dielectric layer;

a first diffusion barrier formed against via and trench vertical sidewalls of the dual-damascene type opening;

second diffusion barrier formed against horizontal surfaces of the dual-damascene type opening;

said first diffusion barrier being a different material than said second diffusion barrier; and

an alloy seed layer over said first and second diffusion barriers.

14. An integrated circuit according to Claim 13 wherein said alloy seed layer comprises copper and at least one

of tantalum and chromium.

15. An integrated circuit comprising:

a substrate;

a first dielectric layer over said substrate;

at least one trench in said first dielectric layer;

a liner comprising a conductive material within said at least one trench;

a first conductive region comprising copper within said at least one trench;

a diffusion barrier and cap layer comprising a metal and a conductive oxide of said metal over said first conductive region; and

a second dielectric layer formed over said first conductive region and said diffusion barrier and cap layer.

16. An integrated circuit according to Claim 15 wherein said diffusion barrier and cap layer comprises Ru and Ru oxide.

17. An integrated circuit according to Claim 15 further comprising a layer of Ag and a layer of Pd between said diffusion barrier and cap layer, and said first conductive region.